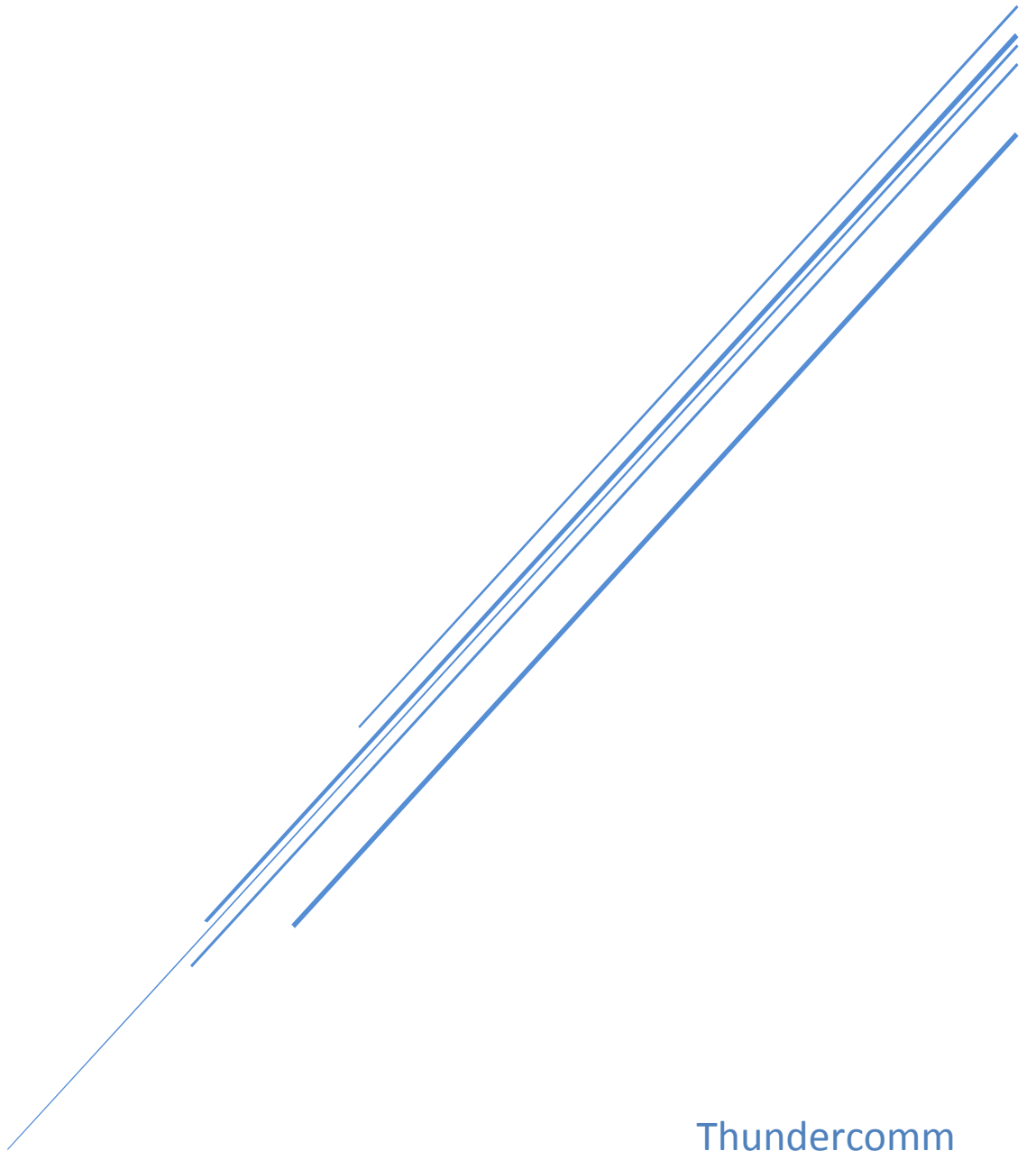


Thundersoft TurboX® S820

SOM Datasheet



Thundercomm

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Version	Date	Description
V0.1	2016-3-18	Initial Version
V0.2	2016-5-16	Update Board to V10
V0.3	2016-6-6	Update connectors pin instruction
V0.4	2016-7-12	Update pin definition: J3001 Pin34: GYRO_INT change to VBATT_CONN_VSENSE_M J3001 Pin44: EN_CHG change to GYRO_INT J3002 Pin34: TX_GTR_THRES change to VREG_L22A_2P8 J2502 Pin2&4: VREG_5V_BST change to VBATT J2502 Pin47&49: PMI_HAP_OUT_P/N change to VBUS_USB_IN J2502 Pin43: FORCE_USB_BOOT change to VPH_PWR
V0.5	2016-7-28	Power consumption Reserve GPS
V0.6	2016-9-19	Update LCD connector manufacture and manufacture part number Update external memory option item Update system block diagram
V0.7	2016-10-21	Update system block diagram Update PIN Names

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V0.8	2017-03-08	Update the pin definition Update the RF performance
V0.9	2017-03-17	Update the connector function and part number, add the information of RF antenna connector Update APQ8096 SOM to V21
V1.0	2017-03-30	Update the GPIOs
V2.1	2017-09-01	Add interface description and Electrical characteristics
V2.2	2017-10-31	Add I2S timing description

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1 Overview

1.1 Abstract

Thundersoft TurboX®S820 is high level performance intelligent module, integrating Android or Linux system, based on Qualcomm APQ8096 processor. It used the advanced 14 nm Fin FET process, customized 64-bit ARMv8-compliant quad-core applications processor, 2.15GHz CPU process performance, integrated a new Adreno 530 graphics processing unit (GPU).

Thundersoft TurboX® S820 support short-range wireless communication through Wi-Fi 802.11 a/b/g/n/ac and BT4.2, and integrates GPS/GLONASS satellite positioning system. Thundersoft TurboX® S820 support 3840*2400@60fps display, it can connect 3 x camera modules, 1080P video smoothly output, and integrating multiple audio and video input/output interfaces. Thundersoft TurboX® S820 provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports two MIPI-DSI, three MIPI-CSI and SOM common standard protocol interfaces such as USB3.0, USB2.0, SPI, PCIE2.1, I2S, SLIMBUS and HDMI.

Thundersoft TurboX® S820 provide convenient and stable system software solution for IOT field, it can be embedded into the device on VR/AR, Drone, Robot, Smart Camera, Routers, and any other connecting fields. The size of Thundersoft TurboX® S820 module is 40mm x 55mm x 5.5mm, weight 18g, with 299PINs.

1.2 Reference Documents

Document
80-NT204-1 MSM8996-APQ8096 DEVICE SPECIFICATION
80-NT204-41 MSM8996 BASEBAND REFERENCE SCHEMATIC
80-NJ118-1 PMI8994-PMI8996 POWER MANAGEMENT IC DEVICE SPECIFICATION

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1.3 Terms and Acronyms

Acronym/Terminology	Description
ADC	Analog-to-digital converter
BER	Bit error rate
BLSP	BAM-based low-speed peripheral
eMMC	Embedded Multimedia Card
GPIO	General Purpose Input/output
GLONASS	GLONASS Global orbiting navigation satellite system
GNSS	Global navigation satellite system
HDMI	High-Definition Multimedia Interface
LPDDR	Low Power Double Data Rate
LCD	Liquid crystal display
MIPI-CSI	Mobile Industry Processor Interface Camera Serial Interface
MIPI-DSI	Mobile Industry Processor Interface Display Serial Interface
MBHC	Multiple button headset control
MPP	Multipurpose pin
NFC	Near field communicator
PMIC	Power Management Integrated Circuit
OSC	Oscillator
PA	Power amplifier
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation

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PM	Power management
PWM	Pulse width modulation
PoP	Package-on-package
SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SLIMbus	Serial Low-power Inter-chip Media Bus
SPI	Serial peripheral interface
SPMI	Serial power management interface
SSC	Snapdragon™ sensor core
TCXO	Temperature-compensated crystal oscillator
SoC	System on Chip
XTAL	Crystal
SDIO	Secure Digital Input / Output
UART	Universal Asynchronous Receiver Transmitter
USB	Universal serial bus
I2S	Inter-IC Sound
I2C	Inter-integrated circuit
WCN	Wireless connectivity network
WLAN	Wireless local area network
SMPS	Switched-mode power supply
SOM	System On Module
ZIF	Zero Insert Force

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2 Introduction

2.1 Key features

The following table shows the detailed features and performance on Thundersoft TurboX® S820.

Processors	
Applications Processor	Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) Two high-performance Kryo cores – gold cluster (2.15 GHz) Two low-power Kryo cores – silver cluster (1.593 GHz)
Digital signal processing	Hexagon DSP with dual-Hexagon vector processor (HVX-512) (target 825 MHz)
Sensor core	Snapdragon™ sensor core (dedicated Q6 low-power island with 512 KB)
Operating System	Android OS 7
Memory	64GB eMMC + LPDDR4 4GB Dual-channel PoP high-speed memory – LPDDR4 SDRAM designed for 1866 MHz clock.
Multimedia	
Display support	2 x 4-lane DSI DPHY 1.2 and HDMI 2.0 (4K60) or 4K60 WFD HDMI up to 3840 x 2160 at 60fps Maximum concurrency configurations

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	3840x2400 or 4096x2160 at 60Hz primary + 3840x2160 or 4096x2160 at 60Hz HDMI 2560 x 1600 at 60 fps primary + 2560 x 1600 at 60fps secondary + 3840 x 2160 at 60fps HDMI
Camera support	Support 3 x 4-lane MIPI_CSI Dual 14-bit ISP 28 MP + 13 MP, 600 MHz each 16 MP30 ZSL with single ISP ABF3 with radius noise reduction, Demosaic4, TNR, ASF2.2, Dual AF, LTM, CAC2, GIC, Pedestal correction, stats upgrades
Video	
Encode	H.264 BP/MP/HP, MPEG-4 SP/ASP, H.263 P0, VP8, HEVC Main Maximum performance 3840x2160 at 30 fps 4096x2160 at 24 fps
Decode	H.264 BP/MP/HP, MPEG-4 SP/ASP, H.263 P0, VC1 SP/MP/AP, MPEG-2 MP, DivX 3.11/4/5/6, VP8, VP9, HEVC Main, HEVCM10* Maximum performance 3840x2160 at 60 fps 4096x2160at 60 fps
Graphics	Adreno 530 3D graphics accelerator 624 MHz Support by A530 for all important GPU APIs

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	DirectX 12 _FL12 (future-proof DX) OpenGL ES 3.1*+AEP1 and Vulkan OpenCL 2.0*(full), RenderScript Support for 64-bit virtual addresses, allowing for SVM with 64-bit CPUs Supports GPU virtualization
Audio (build in Thundersoft TurboX® S820 Carrier Board)	
Codec	Seven DACs, seven outputs Six differential analog inputs with dedicated ADCs Six digital microphones Snapdragon™ voice activation (SVA) subsystem for ultra low voice wake-up MBHC, ANC 130 dB dynamic range, 24-bit DAC 44.1 kHz native playback SLIMbus to I2S bridge
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	QCELP, EVRC, EVRC-B, EVRC-WB,EVS, GSM-FR, -EFR, -HR; AMR-NB, -WB
Audio Encoders	QCELP, EVRC, AMR-WB, AMR-NB, AAC ELD, AAC and AAC+
Audio Decoders	PCM playback, AAC/AAC+/eAAC+, MP3, WMA (v9 and v10), WMA Lossless, WMA Pro10, AMR-NB, AMR-WB, AMR-WB+, FLAC, ALAC, Vorbis*, AIFF, APE, AC3, eAC3, M8

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Enhanced audio	Surround sound: DTS-HD; DTS express 7.1 Fluence noise cancellation; enhanced speaker protection QAudioFX/Qconcert/QEnsemble
Wireless connectivity	
WLAN	2.4G/5G, support 802.11 a/b/g/n/ac, 2 X 2 MIMO Support AP mode
Bluetooth	Support Bluetooth 4.2 + HS BLE, Backwards compatible with Bluetooth 1.2, 2.X + enhanced data rate.
GNSS	Support GPS/GLONASS (Reserved)
Connectivity	
USB	Two – one USB 2.0 high-speed and one USB 3.0 super-speed/USB 2.0 high-speed Compliant
HDMI	Integrated HDMI Tx core and HDMI PHY Rev 2.0 1080p at 60 Hz refresh; 24-bit RGB color 4k 60 fps HDMI 2-channel Linear Pulse-Code Modulation (LPCM) 8-channel LPCM 24 bit/192 kHz
PCIe	1x PCIe, PCIe v2.1 PHY and 2.1 controller
SDIO	2 x 4-bit, SD 3.0

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	SDC2 is dual-V SD/MMC card, eMMC NAND, eSD/eMMC boot
BLSP	Can be configured as 2 x SPI or 3 x I2C or 5 x UART
UART	up to 4 MHz
I2C	Sensors etc
SPI	Sensors etc
SLIMbus	One, highly multiplexed, high-speed, baseline WCD9335
MI2S	Full duplex stereo or up to quad channel Tx/Rx MI2S (x1) Up to 2 channel for multi-channel audio applications (x1)
PCM	Short and long sync PCM support
GPIO	4+ GPIO ports
Others	
ADC Interface	Support ADC interfaces used for input voltage sense, battery temperature detection and general purpose ADC
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
Physical size	Size: 40mm x 55mm x 5.5mm

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	Weight: approx.18g Interface: Connector
Operating temperature	-10C ~ 70C
RoHS	All hardware components are fully compliant with EU RoHS directive

Table 2.1-1 Detailed features and performance

2.2 Hardware Block Diagram

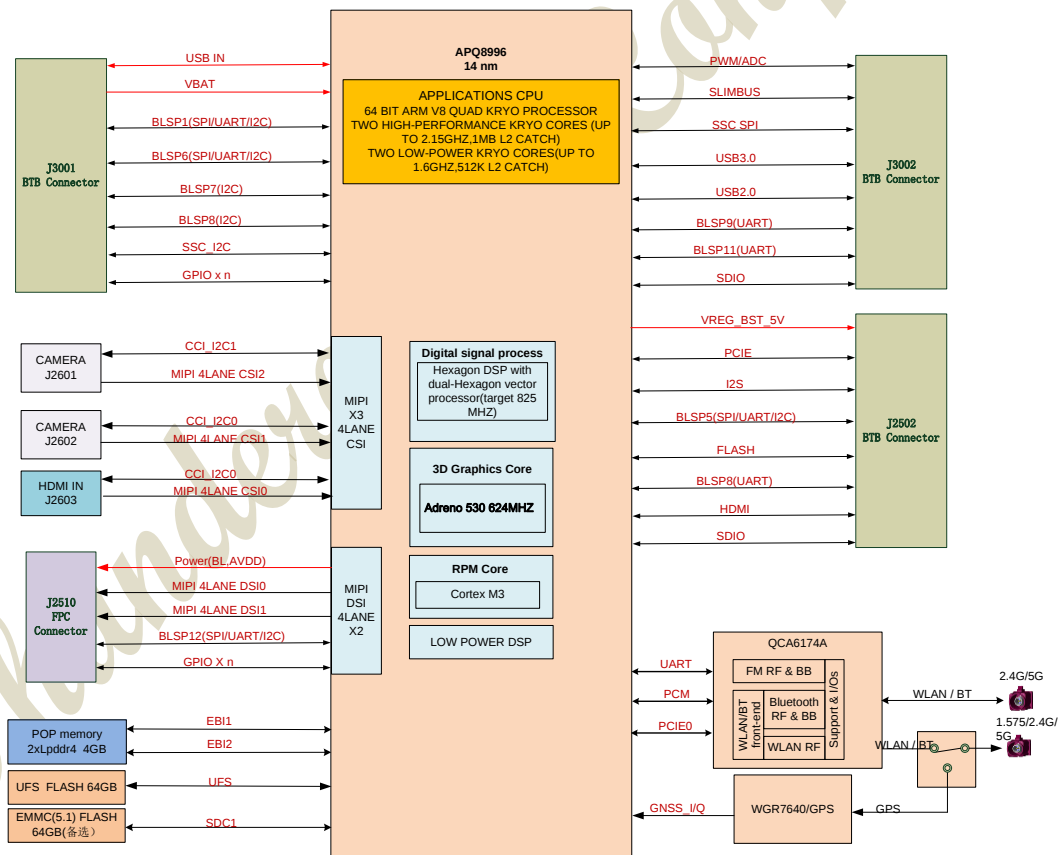


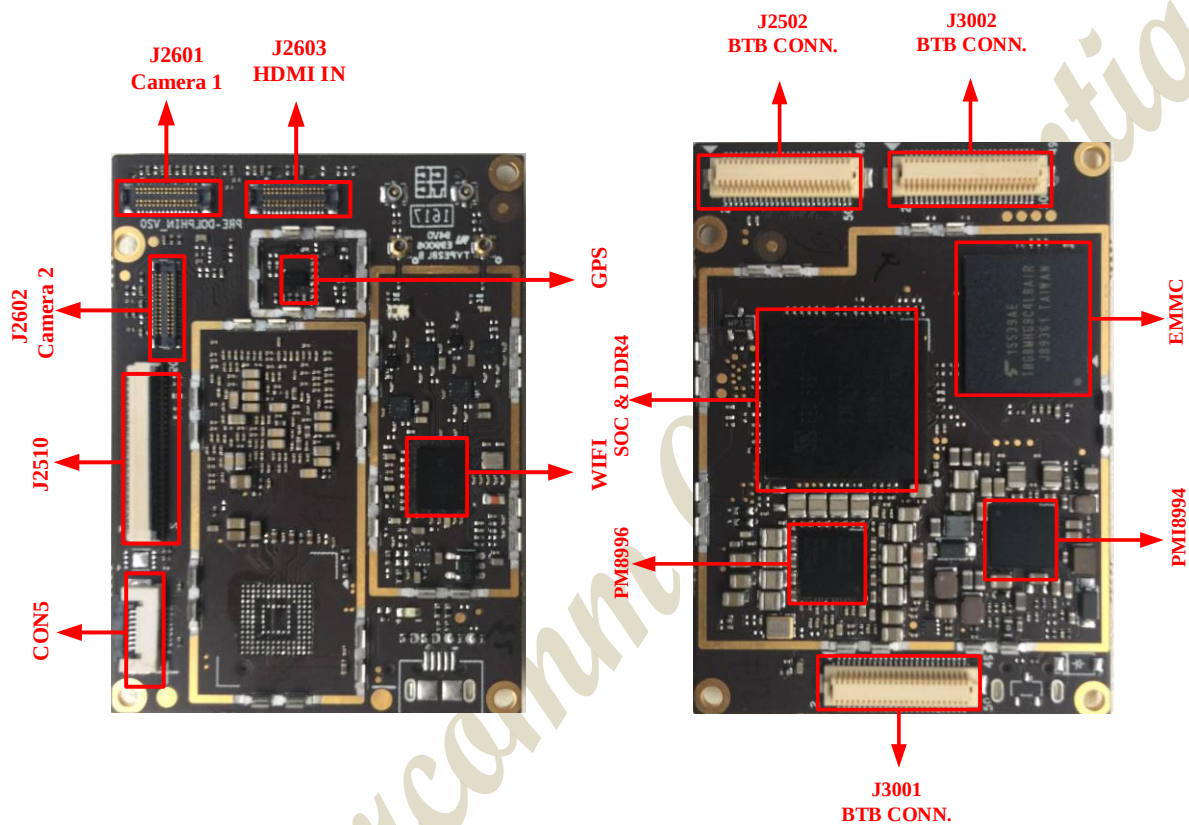
Figure 2.2-1 Thundersoft TurboX® S820 SOM Hardware System Block Diagram

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2.3 Major Components Location

Thundersoft TurboX® S820 SOM’s major components as below map.



ion and Part Number

We have SOM major parts connectors on Thundersoft TurboX® S820. Below map can easy to show the Pin start & end location on connector.

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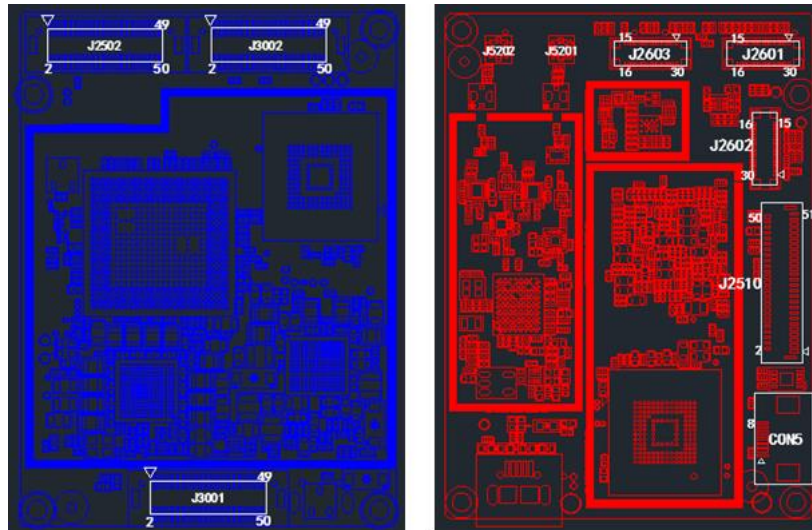


Figure 2.4-1 Thundersoft TurboX® S820 SOM Connector PIN Location

Thundersoft TurboX® S820 SOM Below table indicates connectors detail information.

Part Reference	Description	Manufacturer Part Number	Manufacturer
J2502,J3001, J3002	BTB connectors, used for connecting to Carrier Board.	DF12C(3.0)-50DS-0.5V (81)	HIROSE
J2510	LCD connector, we have reference design for LCD connecting Carrier Board, and Carrier Board connecting to SOM module. You also can connect LCD directly to SOM module if the connector PIN definition is same to LCD connector.	FH35C-51S-0.3SHW(50)	HIROSE
J2601,J2602, J2603	Camera connectors, used for camera module.	GY071-S30	COTEX
J5201,J5202	J5201 is an antenna connector for Wi-Fi/BT/GPS; J5202 is an antenna connector for Wi-Fi.	818000157	ECT
CON5	A ZIF connector, connecting to Carrier Board for the key signals.	SFC-050800H15	SMARTCONN

Table 2.4-1 Connector part number and information

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3 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on Thundersoft TurboX® S820 SOM.

3.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.8 V only)
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_DSI I/O; (1.8 V only)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain

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PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 3, it is 1.8V or 2.95V.
P12	SSC Power group 12, it is 1.8V.

Table 3.1-1 Interfaces parameter definitions

3.2 Interfaces Detail Description

3.2.1 Power Supply Interface

Below table describes all interfaces of SOM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Power Supply					
PIN Name	Location	PIN	Type	Description	Notes
VBATT	J3001	1,3,5,7,9	PI,PO	Power supply in for SOM all operations. Power supply out for battery charging.	
	J2502	2,4			
VBUS_USB_IN	J3001	8,10,12	PI,PO	USB charger input power sources or output during USB-OTG operation. This is a power entry node for the charger and connects to the OVP circuitry.	
	J2502	47,49			
VREG_LVS2A_1P8	J3001	15	PO	Low voltage switch supply output for sensor	
VREG_S4A_1P8	J3001	16	PO	SMPS power output for external	

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				CODEC ; Also can used for 1.8V IO pull up voltage;	
VPH_PWR	J3001	17	PO	Power supply for external equipment out of SOM, which same with internal sequence.	
	J2502	43			
VREG_L21A_2P95	J3001	18	PO	Power output for SD card	
VREG_L22A_2P8	J3002	34	PO	3.3V LDO power output,150mA	
VREG_L19A_3P0	J2502	8	PO	Power output for Sensor	
VREG_L23A_2P8	J2601	4	PO	Cameras AF VDD power supply	
	J2602	4			
	J2603	4			
VREG_LVS1A_1P8	J2601	5	PO	Cameras IO power supply	
	J2602	5			
	J2603	5			
VREG_L17A_2P7	J2601	9	PO	Camera1 AVDD power supply	
VREG_L3A_1P1	J2601	10	PO	Camera1 DVDD power supply	
VREG_L16A_2P7_RCM	J2602	9	PO	Camera2 AVDD power supply	
VREG_WTR_1P0	J2602	10	PO	Cameras DVDD power supply	
	J2603	10			
VREG_L29A_2P8	J2603	9	PO	Camera3 AVDD power supply	
VREG_DISN	J2510	36	PO	LCD negative analog power supply	
VREG_DISP	J2510	37	PO	LCD positive analog power supply	
VREG_L14A_1P8	J2510	38	PO	LCD 1.8V power supply	
VREG_L18A_2P85	J2510	39	PO	Reserved power supply(can be configured)	
VREG_WLED	J2510	41,42	PO	Backlight boost output(max 28.5V)	
GND	J3001	11,13,45,2,4,6,14,20,40	GND		
	J3002	15,37,43,49,18,46	GND		
	J2502	1,7,13,19,6,26,32,38,44,50	GND		
	J2601	1,2,7,13,15,18,21,24,27,30	GND		
	J2602	1,2,7,13,15,18,21,24,27,30	GND		
	J2603	1,2,7,13,15,1	GND		

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		8,21,24,27,30			
	J2510	1,4,7,10,13,1 6,19,22,25,28 ,31,40,47	GND		
	CON5	2,8	GND		

Table 3.2-1 Power Supply Definition

3.2.2 Touchscreen Interface

Touchscreen panels are supported using I2C busses and GPIOs configured as discrete digital inputs.

Touchscreen						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
TP_I2C_SDA	J2510	48	P3	OD	BLSP12 I2C signals	
TP_I2C_SCL	J2510	49	P3	OD	BLSP12 I2C signals	
BLSP12_UART_TX	J2510	50	P3	DO	BLSP12 UART signals	TP-RST
BLSP12_UART_RX	J2510	51	P3	DI	BLSP12 UART signals	TP-INT

Table 3.2-2 Touchscreen interfaces definition

3.2.3 Display Interface

The SOM supports dual 4-lane MIPI_DSI interfaces. 60fps, Up to 4096 x 2160.

Display						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
MIPI_DSIO_LANE3_N	J2510	2	DSI	AO	MIPI0 signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSIO_LANE3_P	J2510	3	DSI	AO		
MIPI_DSIO_LANE2_N	J2510	5	DSI	AO		
MIPI_DSIO_LANE2_P	J2510	6	DSI	AO		
MIPI_DSIO_CLK_N	J2510	8	DSI	AO		
MIPI_DSIO_CLK_P	J2510	9	DSI	AO		
MIPI_DSIO_LANE1_N	J2510	11	DSI	AO		
MIPI_DSIO_LANE1_P	J2510	12	DSI	AO		
MIPI_DSIO_LANE0_N	J2510	14	DSI	AO		
MIPI_DSIO_LANE0_P	J2510	15	DSI	AO		

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MIPI_DSI1_LANE3_N	J2510	17	DSI	AO	MIPI1 Signals for MIPI LCM Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSI1_LANE3_P	J2510	18	DSI	AO		
MIPI_DSI1_LANE2_P	J2510	20	DSI	AO		
MIPI_DSI1_LANE2_N	J2510	21	DSI	AO		
MIPI_DSI1_CLK_P	J2510	23	DSI	AO		
MIPI_DSI1_CLK_N	J2510	24	DSI	AO		
MIPI_DSI1_LANE1_P	J2510	26	DSI	AO		
MIPI_DSI1_LANE1_N	J2510	27	DSI	AO		
MIPI_DSI1_LANE0_N	J2510	29	DSI	AO		
MIPI_DSI1_LANE0_P	J2510	30	DSI	AO		
LCD_RESET_2	J2510	32	P3	DO	LCD reset signal	
LCD_CABC	J2510	33	PWM	DI	LCD PWM input signal	
LCD_RST_N	J2510	34	P3	DO	LCD reset signal	
LCD_TE0	J2510	35	P3	DI	LCD TE signal input	

Table 3.2-3 Display interfaces definition

3.2.4 Display $\pm$ Bias Interface

The SOM supports AMOLED display panel (user-settable hardware/software configuration), which have programmable positive and negative display bias for AMOLED display.

Display $\pm$ Bias						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
VREG_DISN	J2510	36	-5.5V default	PO	negative output voltage	
VREG_DISP	J2510	37	+5.5V default	PO	positive output voltage	

Table 3.2-4 Display Bias interfaces definition

3.2.5 Display Backlighting Interface

The SOM supports White LEDs (WLED) generating backlight for the LCD. The PMIC supports WLEDs with a boost converter that generates the high voltage, which can through 8 LEDs in series or 4 output drivers for sinking the current from WLED strings, each support a string of up to 8 LEDs, and up to 30 mA each.

Backlighting PINs

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PIN Name	Location	PIN	Voltage	Type	Description	Notes
VREG_WLED	J2510	41,42		PO	Backlight boost output(max 28.5V)	
LCD_BL_LED_K1	J2510	43		AI	Backlight low-side current sink input	
LCD_BL_LED_K2	J2510	44		AI		
LCD_BL_LED_K3	J2510	45		AI		
LCD_BL_LED_K4	J2510	46		AI		

Table 3.2-5 Display backlight interface definition

3.2.6 Camera Interfaces

The SOM supports 3 x 4-lane camera interfaces. Camera module should connect J2601 J2602 J2603 socket connector separately.

Camera1 Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA0	J2601	3	P3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL0	J2601	6	P3	OD	CCI0 Clock signal, already pull up on SOM	
MCAM_PWDN	J2601	8	P3	DO	Camera power down signal	
MCAM_RST	J2601	11	P3	DO	Camera reset signal	
MCAM1_STOBE	J2601	12	P3	DI	Camera STROBE signal	
CAM_MCLK0	J2601	14	P3	DO	Camera main clock output	
MIPI_CSIO_LANE3_P	J2601	16	CSI	AI	MIPI Signals of Camera0 Compliant with MIPI Alliance Standard Specification	
MIPI_CSIO_LANE3_N	J2601	17	CSI	AI		
MIPI_CSIO_LANE2_P	J2601	19	CSI	AI		
MIPI_CSIO_LANE2_N	J2601	20	CSI	AI		
MIPI_CSIO_LANE1_P	J2601	28	CSI	AI		
MIPI_CSIO_LANE1_N	J2601	29	CSI	AI		
MIPI_CSIO_LANE0_P	J2601	22	CSI	AI		
MIPI_CSIO_LANE0_N	J2601	23	CSI	AI		
MIPI_CSIO_CLK_P	J2601	25	CSI	AI		
MIPI_CSIO_CLK_N	J2601	26	CSI	AI		

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Camera2 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA0	J2601	3	P3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL0	J2601	6	P3	OD	CCI0 Clock signal, already pull up on SOM	
SMCAM1_POWDN	J2602	8	P3	DO	Camera power down signal	
SMCAM_RESET	J2602	11	P3	DO	Camera reset signal	
SMCAM_STOBE	J2602	12	P3	DI	Camera STROBE signal	
CAM_MCLK1	J2602	14	P3	DO	Camera main clock output	
MIPI_CSI1_LANE3_P	J2602	16	CSI	AI	MIPI Signals of Camera1 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI1_LANE3_N	J2602	17	CSI	AI		
MIPI_CSI1_LANE2_P	J2602	19	CSI	AI		
MIPI_CSI1_LANE2_N	J2602	20	CSI	AI		
MIPI_CSI1_LANE1_P	J2602	28	CSI	AI		
MIPI_CSI1_LANE1_N	J2602	29	CSI	AI		
MIPI_CSI1_LANE0_P	J2602	22	CSI	AI		
MIPI_CSI1_LANE0_N	J2602	23	CSI	AI		
MIPI_CSI1_CLK_P	J2602	25	CSI	AI		
MIPI_CSI1_CLK_N	J2602	26	CSI	AI		

Camera3 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA1	J2603	3	P3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL1	J2603	6	P3	OD	CCI0 Clock signal, already pull up on SOM	
SCAM_PWDN	J2603	8	P3	DO	Camera power down signal	
SCAM_RESET_N	J2603	11	P3	DO	Camera reset signal	
SCAM_STOBE	J2603	12	P3	DI	Camera STROBE signal	
CAM_MCLK2	J2603	14	P3	DO	Camera main clock output	
MIPI_CSI2_LANE3_P	J2603	16	CSI	AI	MIPI Signals of Camera2	
MIPI_CSI2_LANE3_N	J2603	17	CSI	AI		
MIPI_CSI2_LANE2_P	J2603	19	CSI	AI		

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MIPI_CSI2_LANE2_N	J2603	20	CSI	AI	Compliant with MIPI Alliance Standard Specification	
MIPI_CSI2_LANE1_P	J2603	28	CSI	AI		
MIPI_CSI2_LANE1_N	J2603	29	CSI	AI		
MIPI_CSI2_LANE0_P	J2603	22	CSI	AI		
MIPI_CSI2_LANE0_N	J2603	23	CSI	AI		
MIPI_CSI2_CLK_P	J2603	25	CSI	AI		
MIPI_CSI2_CLK_N	J2603	26	CSI	AI		

Table 3.2-6 Camera interface definition

3.2.7 Camera Flash Interface

The SOM supports Flash LED. The flash driver is high current. Two LED channels, independent current control, 12.5 mA step size.

Flash interfaces						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
FLASH_LED1	J2502	10		AO	Power supply for flashlight 1, connect to positive port	
FLASH_LED2	J2502	12		AO	Power supply for flashlight 2, connect to positive port	

Table 3.2-7 Camera Flash interface definition

3.2.8 Audio Interface

The SOM provide SLIMBUS and I2S interfaces for audio. SLIMBUS interface is dedicate for external codec IC, which can build system's audio functions. I2S interface can connect audio devices.

Audio Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
SLIMBUS_DATA0	J3002	36	P3	IO	Slimbus, connect to COEDC Compliant with MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	
SLIMBUS_DATA1	J3002	38	P3	IO		
SLIMBUS_CLK	J3002	40	P3	DO		

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MI2S3_DO	J2502	21	P3	DO	I2S signals Compliant with Philips I2S Bus Specifications	
MI2S3_DI	J2502	35	P3	DI		
MI2S3_MCLK	J2502	23	P3	DO		
MI2S3_SCK	J2502	33	P3	DO		
MI2S3_WS	J2502	45	P3	DO		
CODEC_INT1	J3002	30	P3	DI	CODEC interrupt signal	
CODEC_INT2	J3002	32	P3	DI		
CODEC_RESET_N	J3002	42	P3	DO	CODEC reset signal	
DIVCLK1_CDC	J3002	44	P3	DO	CODEC clock	

Table 3.2-8 Audio interface definition

3.2.9 USB Interface

The SOM support USB host and slave. Dual USB port support, one is USB 2.0 high-speed, the other is USB 3.0 super-speed/USB 2.0 high-speed compliant

SS/HS USB (3.0/2.0) Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
USB3_SS_TX0_P	J3002	39		DO	USB 3.0 Signals Compliant with USB 3.1 standard specification	
USB3_SS_TX0_M	J3002	41		DO		
USB3_SS_RX0_P	J3002	45		DI		
USB3_SS_RX0_M	J3002	47		DI		
USB_HS_DP	J3001	47		IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	Require differential impedance of 90Ω.
USB_HS_DM	J3001	49		IO		
VBUS_USB_IN	J3001 J2502	8,10,12 47,49		PI		
HS USB (2.0) Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
USB_ID	J3001	43		AI		
USB2_HS_DP	J3002	48		IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	
USB2_HS_DM	J3002	50		IO		
VBUS_USB_IN	J3001	8,10,12		PI		

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	J2502	47,49				
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Table 3.2-9 USB interface definition

3.2.10 HDMI Interface

The SOM support one HDMI2.0 output interface. Complete 4K 60fps entertainment system, also supports the audio portion of HDMI using MSM-internal connections.

HDMI Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
HDMI_CEC	J2502	18	P3	IO	HDMI Signals Compliant with HDMI Specification Version 2.0	
HDMI_DDC_CLK	J2502	20	P3	OD		
HDMI_DDC_DATA	J2502	22	P3	OD		
HDMI_HPD_CON	J2502	24	P3	DI		
HDMI_TX2_M	J2502	28		AO		
HDMI_TX2_P	J2502	30		AO		
HDMI_TX0_M	J2502	34		AO		
HDMI_TX0_P	J2502	36		AO		
HDMI_TX1_P	J2502	40		AO		
HDMI_TX1_M	J2502	42		AO		
HDMI_TCLK_P	J2502	46		AO		
HDMI_TCLK_M	J2502	48		AO		

Table 3.2-10 HDMI interface definition

3.2.11 PCIe Interface

The SOM support one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

PCIe Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
PCIE1_REFCLK_N	J2502	3		AO	PCIe Signals Compliant with PCI Express Specification Revision 2.1	
PCIE1_REFCLK_P	J2502	5		AO		
PCIE_MSM_RX_N	J2502	9		AI		
PCIE_MSM_RX_P	J2502	11		AI		
PCIE1_MSM_TX_N	J2502	15		AO		

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PCIE1_MSM_TX_P	J2502	17		AO		
PCIE1_CLKREQ_N	J2502	29	P3	DI	PCie clock require signal, need to reserve pull up resistor	
PCIE1_RST_N	J3001	35	P3	DO	PCie reset signal	
PCIE1_WAKEUP	J3001	37	P3	DI	PCie wake up signal	

Table 3.2-11 PCie interface definition

3.2.12 SSC Interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode. The SSC has a dedicated 512 kB L2 cache.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

SSC Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
SSC_I2C_3_SDA	J3001	31	P12	OD	These I2C signals are dedicated to Sensor	
SSC_I2C_3_SCL	J3001	33	P12	OD		
SSC_I2C_2_SDA	J3001	28	P12	OD	These I2C signals are dedicated to Sensor	
SSC_I2C_2_SCL	J3001	30	P12	OD		
SSC_SPI_1_CLK	J3002	1	P12	DO	Snapdragon™ Sensor Core SPI signals	
SSC_SPI_1_MOSI	J3002	3	P12	DO		
SSC_SPI_1_CS_N	J3002	5	P12	DO		
SSC_SPI_1_MISO	J3002	7	P12	DI		

Table 3.2-12 SSC interface definition

3.2.13 SDIO Interface

The SOM support dual 4-laneSDIO, SDC2 connect to SD-card.

The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 Mhz.

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- The signals routing should be 50ohm±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

SDIO (SDC2) Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
SDC2_SDCARD_CLK	J3002	17	P2	DO	SD card signals; SD_CARD_DET_N need pull up to P3	
SDC2_SDCARD_CMD	J3002	19	P2	IO		
SDC2_SDCARD_D3	J3002	21	P2	IO		
SDC2_SDCARD_D2	J3002	23	P2	IO		
SDC2_SDCARD_D1	J3002	25	P2	IO		
SDC2_SDCARD_D0	J3002	27	P2	IO		
SD_CARD_DET_N	J3002	29	P3	DI		

SDIO (SDC4) Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
SDC4_D0	J3002	10	P3	IO	SDIO Signals Compliant with SDIO standard specification.	
SDC4_D1	J3002	14	P3	IO		
SDC4_D2	J3002	22	P3	IO		
SDC4_D3	J3002	12	P3	IO		
SDC4_CLK	J3002	20	P3	DO		
SDC4_CMD	J3002	16	P3	IO		

Table 3.2-13 SDIO interface definition

3.2.14 BLSP Interface

These GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, SPI, or I2C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus is supplemented by a 2.2kΩ pull-up resistor

BLSP Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
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BLSP6_UART_TX	J3001	23	P3	IO	BLSP6 can be configured to GPIO or UART or SPI or I2C	
BLSP6_UART_RX	J3001	25	P3	IO		
BLSP6_I2C_SDA	J3001	27	P3	IO		
BLSP6_I2C_SCL	J3001	29	P3	IO		
APPS_I2C7_SDA	J3001	24	P3	IO	BLSP7 can be configured to GPIO or I2C	
APPS_I2C7_SCL	J3001	26	P3	IO		
NFC_SPI_ESE_MOSI	J3002	31	P3	IO	BLSP1 can be configured to GPIO or UART or SPI or I2C	
NFC_SPI_ESE_MISO	J3002	33	P3	IO		
NFC_SPI_ESE_CLK	J3002	35	P3	IO		
NFC_SPI_ESE_CS	J3002	28	P3	IO		
BLSP9_UART_TX	J3002	2	P3	IO	BLSP9 can be configured to GPIO or UART	
BLSP9_UART_RX	J3002	4	P3	IO		
BLSP11_UART_TX	J3002	24	P3	IO	BLSP11 can be configured to GPIO or UART	
BLSP11_UART_RX	J3002	26	P3	IO		
FP_SPI_CS	J2502	25	P3	IO	BLSP5 can be configured to GPIO or UART or SPI or I2C	
FP_SPI_MOSI	J2502	27	P3	IO		
FP_SPI_MISO	J2502	31	P3	IO		
FP_SPI_CLK	J2502	37	P3	IO		

Table 3.2-14 BLSP interface definition

3.2.15 Power on Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s powering on system. Power on/off key signal can be connected to ground through J3001.41 or CON5.1; the other power on method is: when using CBL_PWR_N pin connect to ground, insert battery or power supply, SOM will power on automatically.

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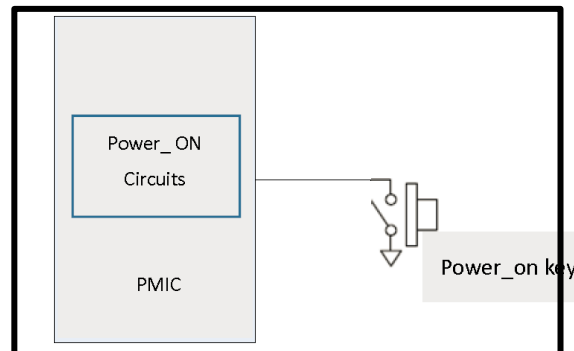


Figure 3.2-1 Power on signal

Power on Interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
KYPD_PWR_N1	J3001	41	pulled up internally through a 200K resistor to 1.8V	DI	Power on/off key signal,	Low level active
	CON5	1				
CBL_PWR_N	J3002	9	pulled up internally through a 200K resistor to 1.8V	DI	Signal use for auto power on when you plug in a battery, active low, internal pull up	

Table 3.2-15 Power on interface definition

3.2.16 Reset Interface

Extended press of volume key will initiate a shutdown or reset (software selectable)

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long key press of PM_RESIN_N, or KYPD_PWR_N1, or PM_RESIN_N + KYPD_PWR_N1.

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The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers

Reset Pin						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
PM_RESIN_N	J3001	39	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	
	CON5	3				

Table 3.2-16 Reset interface definition

3.2.17 Keys Interface

KEY_GPIO can be configure to key functions as your request.

KEYs PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
KEY_VOL_UP_N	CON5	4	P3	DI	Volume up key signal, Low active	
KEY_HOME_N	CON5	5	P3	DI	Home(can be configured) key signal, Low active	
KEY_BACK_N	CON5	6	P3	DI	Back(can be configured) key signal, Low active	
KEY_GPIO	CON5	7	P3	DI	Reserved(can be configured), Low active	

Table 3.2-17 Keys interface definition

3.2.18 Sensor Interrupt Interface

All these interfaces dedicate to below sensors.

Sensor Interrupt PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
ALPS_INT_N	J3001	19	P3	DI	Ambient light sensor interrupt signal	
FP_INT	J3001	21	P3	DI	9-xia Sensor interrupt signal	
MAG_DRDY_INT	J3001	22	P3	DI	Gesture sensor interrupt	

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GYRO_INT	J3001	44	P3	DI	GYRO Sensor interrupt	
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Table 3.2-18 Sensor interrupt definition

3.2.19 Debug UART Interface

This is interface dedicate for debug.

Debug UART PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
MSM_UART_TX	J2502	39	P3	DO	BLSP8 UART signals, can use for debug	
MSM_UART_RX	J2502	41	P3	DI		

Table 3.2-19 Debug UART interface definition

3.2.20 Battery Interface

This is dedicate for battery interface, major for monitoring battery status, inserting, voltage detect, and charging.

Battery PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
VBATT_CONN_VSENSE_P	J3001	32	VBATT	AI	Battery voltage sense positive input signal	
VBATT_CONN_VSENSE_M	J3001	34	VBATT	AI	Battery voltage sense negative input signal	
RSENSE_EXT_M	J3001	36	VBATT	AI	Battery current sense negative input signal	
RSENSE_EXT_P	J3001	38	VBATT	AI	Battery current sense positive input signal	
BAT_THERM	J3001	42	2.7V	AI	Battery temperature sense input signal	

Table 3.2-20 Battery interface definition

3.2.21 Parallel Charging Interface

The SOM keeps below PINs connecting with external SMB IC for parallel charging.

- Efficiency is improved due to reduction in DC losses at high charging currents.

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- Splitting current between two circuits helps spread and dissipate the heat and splits the dominant hot spot.
- Thermal performance is greatly improved compared to a single charger solution.

Other Interfaces						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
PARALLEL_CHG_EN	J3001	46	P3	DO	Parallel charge enable signal	
PARALLEL_CHG_SHDN	J3001	48	VCHG	DO	Parallel charge shut down signal	
SMB1351_VCHG	J3001	50	P3	DI	SMB1351 charging state indicated signal	

Table 3.2-21 Parallel Charging interface definition

3.2.22 MPPs Interface

Any MPP can be configured as ADC, current sink.

The ADC input cannot reliably go below 0.05V or above (P3 – 0.05 V); do not exceed this range.

Programmable current sink for driving LEDs.

MPPs PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
PMI_MPP1	J3002	11		DO	Can be configured as LPG PWM	
PM_MPP5	J3002	13		IO	Can be configured as current sink	

Table 3.2-22 MPPs interface definition

3.2.23 PWMs and LED Current Driver Interface

The SOM support dual PWM output and dual LED Current Driver, all PWM output by Light Pulse Generators.

LED Current Driver PINs can be used for different events, they are separate controller. Independently programmable duty cycle and period via LPGs (6-or 9-bit resolution) for digital dimming.

Flash or blinking with register-selectable durations of ON-time from 0 to 1 second in ≤ 0.05 -second steps, and flashing periods from 0 to 12 seconds in steps of ≤ 0.5 seconds (or always on).

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PWMs PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
PM_PWM1	J3002	6	P3	IO	Can be configured as GPIO and PWM(max 4MHz)	LPG bank1
PM_PWM2	J3002	8	P3	IO		LPG bank2
LED Driver PINs						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
GREEN_LED	J2502	14		AO	Custom indicator light, connect to positive port	LPG bank1
RED_LED	J2502	16		AO	Custom indicator light, connect to positive port	LPG bank0

Table 3.2-23 PWMs and LED Current Driver interface definition

3.2.24 Antenna Interface

The SOM provides the fully-integrated WLAN, Bluetooth and GPS function.

The WLAN, Bluetooth and GPS share the antenna port with 50ohm impedance.

- WLAN supports 2 × 2 multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards.
- Supports Bluetooth 4.2 + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.
- Supports GPS, GLONASS, and COMPASS operation.

Antenna interface						
PIN Name	Location	PIN	Voltage	Type	Description	Notes
Antenna 1	J5201			IO	Antenna 1 supports WIFI 2.4G/5G & BT & GPS	Chain0
Antenna 2	J5202			IO	Antenna 2 supports WIFI 2.4G/5G	Chain1

Table 3.2-24 Antenna interface definition

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4.1 Absolute Maximum Ratings

The SOM needs to be desinged in the operatin conditons which is shown as below table.

Parameter	Min	Max	Units
Input Power voltage			
VBUS_USB_IN	-0.3	20	V
VBAT	-0.5	6	V
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.5	6	V
ESD			
ESD-HBM model rating		±2k	KV
ESD-CDM model rating		±4k	KV

Table 4.1-1 Absolute rating condition

Notes: for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial Production stage.

4.2 Operating Conditions

The SOM needs to be desinged in the operatin conditons which is shown as below table.

Parameters	Min	Typical	Max	Units
Input Power voltage				
VBUS_VBUS_IN	+3.7	5	+10	V
VBAT	+3.6	3.8	+4.35	V
VBAT	3			A
VBATT_CONN_VSENSE_P,	+3.6	3.8	+4.35	V

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VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P					
Thermal conditions					
Operating temperature	-10	25	70	°C	
Storage temperature	-40	-	80	°C	

Table 4.2-1 Operating condition

Note: For the thermal conditons, operatin and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.

4.3 Output Power

The SOM provide power supply for external device, like camera module, SD card, LCD module, and so on. Below map show the details.

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Default ON	Expected use
VREG_LVS2A_1P8	+1.8	+1.7-- +1.95	100	N	supply output for sensor
VREG_S4A_1P8	+1.8	NA	300	Y	SMPS power output for extra position CODEC, and 1.8V IO pull up voltage;
VPH_PWR	+4.2	+3.6-- +4.35	600	N	for external device requested power on sequence Each Pin is 300mA
VREG_L21A_2P95	+2.95	+1.62--+3.6	300	Y	Power output for SD card
VREG_L22A_2P8	+2.8	+1.62--+3.6	150	N	3.3V LDO power output,150mA
VREG_L19A_3P0	+3.0	+1.62--+3.6	300	N	Power output for Sensor

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VREG_L23A_2P8	+2.8	+1.62--+3.6	600	N	Cameras AF VDD power supply Each Pin 300mA
VREG_LVS1A_1P8	+1.8	+1.7--+1.95	300		Cameras IO power supply
VREG_L17A_2P7	+2.7	+1.62--+3.6	300		Camera1 AVDD power supply
VREG_L3A_1P1	+1.1	+0.9--+1.3	300		Camera1 DVDD power supply
VREG_L16A_2P7_RCM	+2.7	+2.56--+3.6	150		Camera2 AVDD power supply
VREG_WTR_1P0	+1.0	+0.9--+1.3	300		Cameras DVDD power supply
VREG_L29A_2P8	+2.8	+1.62--+3.6	300		Camera3 AVDD power supply
VREG_L14A_1P8	+1.8	+1.62--+3.6	150		LCD 1.8V power supply
VREG_L18A_2P85	+2.85	+1.62--+3.6	300		Reserved power supply(can be configured)

Table 4.3-1 Output power

4.4 Backlight output

White LEDs (WLED) generate backlighting for the handset's LCD. Pertinent performance specifications are listed in Table 4.4-1.

Function	Min	Typ	Max	Units	Expected use
VREG_WLED	+6.0		+28.5	V	Backlight boost output(max 28.5V)
LCD_BL_LED_K1	0		30	mA	Backlight low-side current sink input
LCD_BL_LED_K2	0		30	mA	
LCD_BL_LED_K3	0		30	mA	

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LCD_BL_LED_K4	0		30	mA	
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Table 4.4-1 Backlight output

4.5 Display $\pm$ bias

Pertinent performance specifications are listed in Table 4.5-1 respectively

Function	Default voltage(V)	Load = 100 mA range(V)	Max current(mA)	Default ON	Expected use
VREG_DISN	-5.5	-1.4-- -6.0	150		negative analog power supply for LCD
VREG_DISP	+5.5	+5.0-- +6.1	150		positive analog power supply for LCD

Table 4.5-1 Backlight output

4.6 Flash drivers

This high current driver supports flash and torch modes, pertinent performance specifications are listed in Table 4.6-1.

Function	Min	Typ	Max	Units	Expected use
FLASH_LED1 & FLASH_LED2					
FLASH			600	mA	
Torch			200	mA	
Output current steps		12.5		mA	

Table 4.6-1 Flash driver

4.7 Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage. The SOM IO voltage level is the same with P3 except the SD card and analog input/output. The I2C, USB, MIPI and UART comply with the standards.

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4.7.1 Digital GPIO characteristics

The following table shows the digital GPIO characteristics:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.7* P3	P3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt,	-0.3	0.3* P3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VREG_L5_1P8-0.45	VREG_L5_1P8	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

Table 4.7-1 Digital IO voltage performance

4.7.2 SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.95V. the following table shows the SD card digital I/O characteristics:

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/2.065	-	2.1/3.25	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.45/0.74	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω

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VOH	High-level output voltage	1.4/2.21	-	1.8/2.95	V
VOL	Low-level output voltage	0/0	-	0.225/1.091	V

Table 4.7-2 SD digital IO voltage performance (1.8V/2.95V)

4.8 MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None

Table 4.8-1 MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

Table 4.8-2 MIPI_CSI

4.9 USB

The SOM supports USB standards and exceptions.

Applicable standard	Feature exceptions	APQ variation
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None	None

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Table 4.9-1 USB

4.10 PCIe

The SOM supports PCIe standards and exceptions

Applicable standard	Feature exceptions	APQ variation
PCI Express Specification, Revision 2.1 (March 4, 2009 or later)	None	None

Table 4.10-1 PCIe

4.11 HDMI

The SOM supports HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variation
HDMI Specification Version 2.0	None	None

Table 4.11-1 HDMI

4.12 SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variation
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

Table 4.12-1 SLIMbus

4.13 SDIO

The SOM Supports SD standards and exceptions

Applicable standard	Feature exceptions
Embedded Multimedia Card (eMMC) Specification version 5.1	None

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Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Table 4.13-1 SDIO

4.14 I2S

The SOM I2S standards and exceptions:

Legacy I2S interfaces for primary and secondary microphones and speakers.

The multiple I2S (MI2S) interface for microphone and speaker functions, including 7.1 audio for HDMI.

It supports both master and slave mode.

Supports 16, 24, or 32-bit resolution audio samples

Supports 8, 16, 32, 48, 96 and 192 kHz sampling rate in Master mode, and all standard sample rates in Slave mode.

Supports 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s).

Maximum clock frequency supported 12.288 MHz.

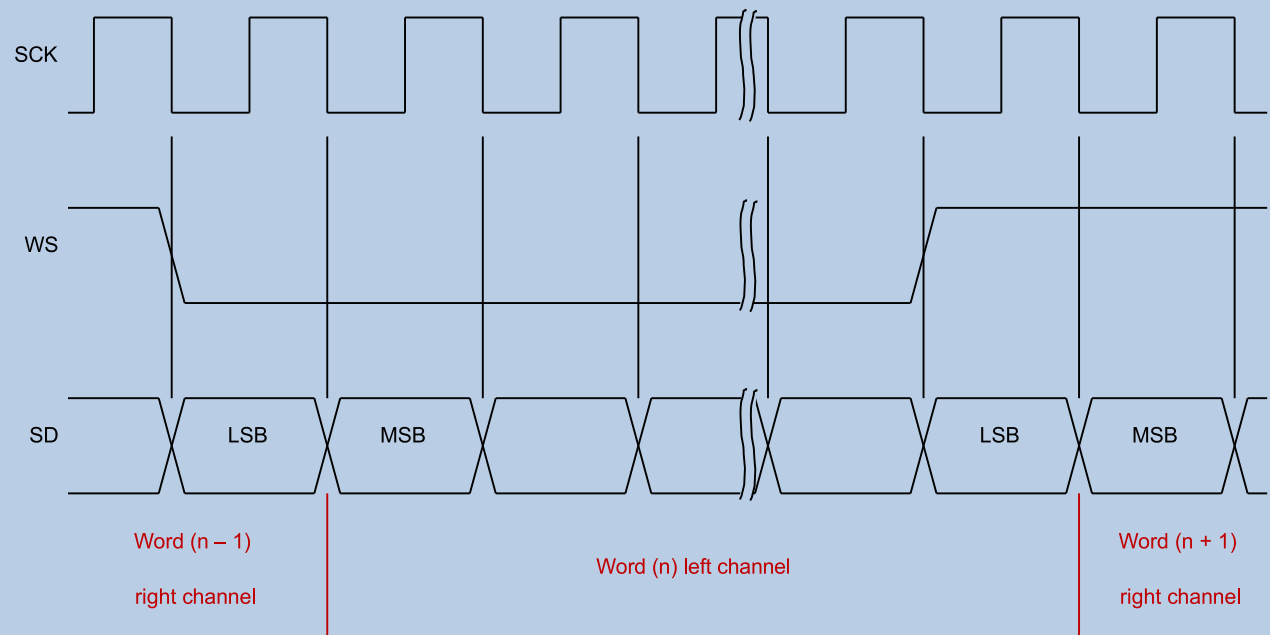
An additional pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Applicable standard	Feature exceptions	MSM variations
Philips I2S Bus Specifications revised June 5, 1996	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.

Table 4.14-1 I2S

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High-level I2S timing



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I2S timing details – Tx and Rx

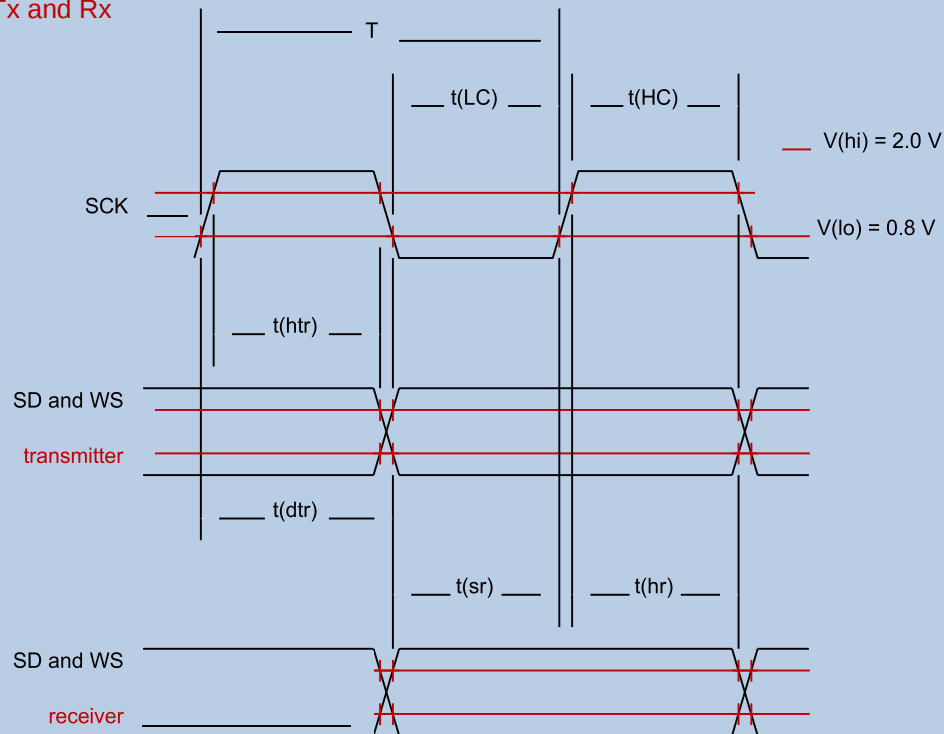


Figure 4.14-1 I2S timing diagram

The word-select signal is a 50% duty cycle signal. Data is delayed 1 bit-clock, relative to the word select.

Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.

I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.

The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high

Parameter	Comments	Min	Typ	Max	Unit
Using internal SCK					
Frequency	—	—	—	12.288	MHz
T	Clock period	81.380	—	—	ns
t(HC)	Clock high	$0.45 \times T$	—	$0.55 \times T$	ns
t(LC)	Clock low	$0.45 \times T$	—	$0.55 \times T$	ns

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t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	$0.45 \times T$	–	$0.55 \times T$	ns
t(LC)	Clock low	–	$0.45 \times T$	–	$0.55 \times T$	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns

Table 4.14-2 I2S Timing

4.15 I2C

The SOM I2C standards and exceptions:

Applicable standard	Feature exceptions
I2C Specification, version 3.0	None

Table 4.15-1 I2C

4.16 SPI

The SOM supports **SPI** standards and exceptions: IT IS supports SPI as a master only.

4.17 Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor.

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Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected. Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Function	Min	Type	Max	Units	Expected use
VBATT_CONN_VSENSE_P & VBATT_CONN_VSENSE_M, RSENSE_EXT_M & RSENSE_EXT_P					
ADC resolution			15	bits	Voltage ADC
			9	bits	ID ADC
			15	bits	Current ADC
ADC clock conversion frequency		200		kHz	

Table 4.17-1 Fuel Gauge

4.18 LED Current Driver

Several types of low-voltage LED current drivers are available: Red, green, drivers that operate off a dedicated supply voltage.

Function	Min	Type	Max	Units	Expected use
RED_LED & GREEN_LED					
Current per channel (I out)			8	mA	
Dimming PWM frequency	0.1		18.75	KHZ	
Dimming Resolution	6		9	bit	

Table 4.18-1 LED current Driver

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4.19 Mpps

MPPs can be configured any of the functions specified within Table 4.19-1

Function	Min	Typ	Max	Units	Expected use
PMI_MPP1 & PM_MPP5					
MPP configured as digital input					
Logic high-input	$0.65 \cdot VM^1$	-	-	V	
Logic low-input	-	-	$0.35 \cdot VM$	V	
MPP configured as digital output					
Logic high-output	$VM - 0.45$	-	VM	V	
Logic low-output	0	-	0.45	V	
Drive strength					
Logic high ($V_M > 2.5\text{ V}$)	5.1	7.3	15.2	mA	
Logic high ($V_M < 2.5\text{ V}$)	3.3	4.9	9.9		
Logic low	5.9	11.3	36.0		
MPP configured as analog input					
Input current	-	-	100	mA	
MPPs configured as current sinks					
Output current	0	-	40	mA	

Table 4.19-1 Mpps

Notes:

VM0 = VPH_PWR.

VM1 = 1.8V

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4.20 Power Consumption

Power Consumption					
S/N	Test Items and Test Condition		UNIT	DUT	
				average value	data range
1	Normal Operation Current (Play Movie) -Wi-Fi off, BT off - Vol Max, no LCD, no Camera	4K	mA	382	245--634
		1080P		305	270--545
2	Normal Operation Current (Idle mode) - Restart the device - At Home Page - No LCD. No Camera	WIFI ON	mA	104	64.7--416
		WIFI OFF	mA	71	63.1--99
3	Normal Operation Current (Sleep Mode) - No LCD. No camera	WIFI ON	mA	24	12.4--239
		WIFI OFF	mA	6	5.3--6.1
4	Normal Operation Current (online Play Movie 1080P Movie) - No LCD. No camera	WIFI On	mA	485	222---989
5	Run in CPU Max Loading(1.5G+2.1G)	WIFI On	mA	2389	1506--3287
6	Camera Record no LCD	WIFI Off	mA	NA	NA
7	Leakage current	-	uA	178	<200uA

Table 4.20-1 Power Consumption (Without LCD/Camera)

4.21 Thermal

This chart records thermal test data, to make sure the SOM working on highest performance, strong suggest make solution for heat sink. Table 4.21-1 describes SOM thermal test point.

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Thermal Test Condition

1	Test case	The test script of CPU + USB + Charging + WIFI open
2	HW Version	DOPHIN_V23, DOLPHIN_IO_v30
3	Test points	CPU +DDR , EMMC , PM8996 , PMI8994 (refer to Figure-2)
4	Ambient temperature	25°C

Table 4.21-1 Thermal Test

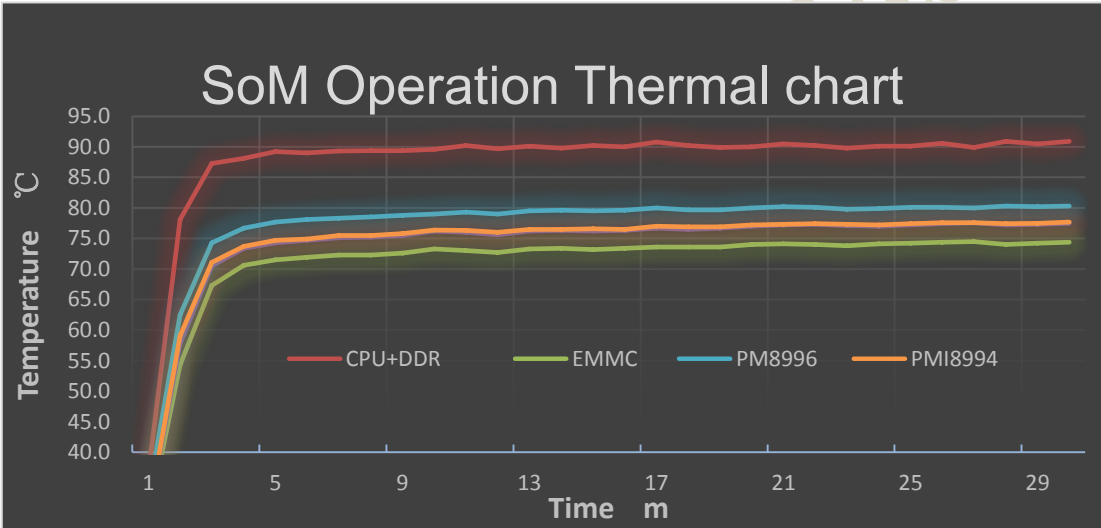


Figure 4.21-1 Thermal Data without Heat Sink Design

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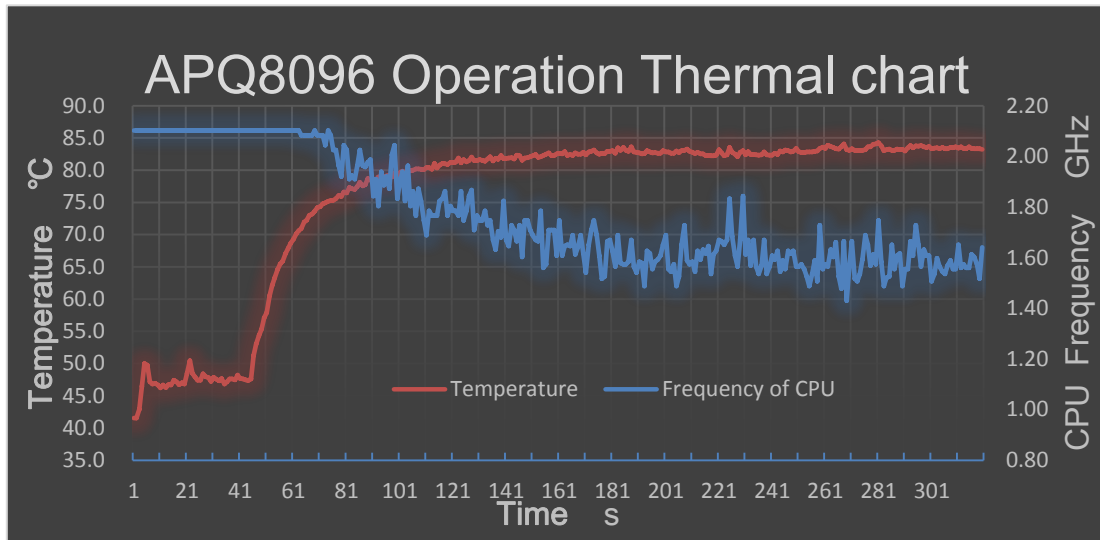


Figure 4.21-2 Frequency of CPU VS Temperature without heat sink design

4.22 RF Performance

4.22.1 Wi-Fi Performance

Wi-Fi supports 2.4G & 5G, below table records the RF performance test result.

2.4G RF Performance					
11M					
Test Item		Expected Result	1	6	11
11b	Transmit Power(dBm)	16±1.5dBm	16.910	16.600	16.610
	Reference sensitivity (PER<8%)	11M<-76dBm	-90	-89	-90
54M					
Test Item		Expected Result	1	6	11
11g	Transmit Power(dBm)	15±1.5dBm	15.970	15.780	15.680

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	Reference sensitivity (PER<10%)	54M<-65dBm	-76	-74	-75
MCS7					
Test Item		Expected Result	1	6	11
11n(20)	Transmit Power(dBm)	14±1.5dBm	15.010	14.760	14.700
	Reference sensitivity (PER<10%)	MCS7<-64dBm	-73	-71	-72
MCS7					
Test Item		Expected Result	3	6	11
11n(40)	Transmit Power(dBm)	14±1.5dBm	14.960	14.920	14.870
	Reference sensitivity (PER<10%)	MCS7<-61dBm	-69	-69	-68

5.8G RF Performance									
54M									
Test Item		Expected Result	36 (5180)	60 (5300)	100 (5500)	120 (5600)	149 (5745)	161 (5805)	165 (5825)
11a	Transmit Power(dBm)	13±1.5dBm	13.710	13.790	13.380	13.670	13.140	13.330	13.320
	Reference sensitivity (PER<10%)	54M<-65dBm	-76	-76	-76	-76	-76	-75	-75

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MCS7									
Test Item		Expected Result	36 (5180)	60 (5300)	100 (5500)	120 (5600)	149 (5745)	161 (5805)	165 (5825)
11n(20)	Transmit Power(dBm)	12±1.5dBm	13.090	13.230	12.940	13.170	12.660	12.810	12.880
	Reference sensitivity (PER<10%)	MCS7≤-64dBm	-73	-74	-73	-73	-73	-72	-73
MCS7									
Test Item		Expected Result	38 (5190)	62 (5310)	102 (5510)	118 (5590)	134 (5670)	151 (5755)	159 (5795)
11n(40)	Transmit Power(dBm)	12±1.5dBm	13.070	13.180	13.000	13.200	13.050	12.750	12.950
	Reference sensitivity (PER<10%)	MCS7≤-61dBm	-71	-71	-70	-70	-70	-70	-69
MCS8									
Test Item		Expected Result	36 (5180)	60 (5300)	100 (5500)	120 (5600)	149 (5745)	161 (5805)	165 (5825)
11ac(20 MHz)	Transmit Power(dBm)	12±1.5dBm	12.790	12.870	12.970	12.780	12.750	12.820	12.970
	Reference sensitivity (PER<10%)	MCS8<-57dBm	-68	-69	-69	-69	-68	-67	-67
MCS9									

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Test Item		Expected Result	38 (5190)	62 (5310)	102 (5510)	118 (5590)	134 (5670)	151 (5755)	159 (5795)
11ac(40 MHz)	Transmit Power(dBm)	10±1.5dBm	10.650	10.800	11.020	10.930	10.860	10.730	10.930
	Reference sensitivity (PER<10%)	MCS9<-54dBm	-65	-65	-65	-65	-65	-64	-63
MCS9									
Test Item		Expected Result	46 (5230)	58 (5290)	110 (5550)	122 (5610)	130 (5650)	155 (5775)	159 (5795)
11ac(80 MHz)	Transmit Power(dBm)	10±1.5dBm	10.640	10.360	10.940	10.960	10.770	10.770	10.880
	Reference sensitivity (PER<10%)	MCS9≤-51dBm	-61	-61	-61	-61	-60	-60	-58

Table 4.22-1 WIFI Performance

4.22.2 BT Performance

BT RF Performance						
Test Equipment : IQ2010/CMW500			RF IN/OUT Offset : 1dB			
Test Item			Expected Result	Channel		
				2402	2440	2480
1	Output Power	Avg(dBm)	-20~20dBm	0.04	0.47	-0.24
2	Initial Carrier Frequency	Offset(KHz)	±75KHz	-23.2	-25.1	-30.2
3	Transmit Spectrum	±500KHZ	<-20dBc	Pass	Pass	Pass

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	mask	2MHZ	<-20dBm	Pass	Pass	Pass
		3MHZ	<-40dBm	Pass	Pass	Pass
4	Modulation Characteristic	Δf1 avg	225 kHz ~ 275 kHz	248.3	247.4	247.7
		Δf2 avg	≥185KHz	271.9	271.5	269.9
5	Carrier Frequency Drift	Drift (kHz)	±40KHz	1.0	1.1	1.1
6	Sensitivity	BER≤0.1%	≤-70dBm	-95	-95	-94

Table 4.22-2 BT Performance

4.22.3 GPS Performance (Reserve)

GPS RF Performance	
Conditions : VBAT=4.0V ; signal source=-130dBm/Hz,Temp:25°C	
C/NO	40dB

Table 4.22-3 GPS Performance

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5 Connector PIN Summary

5.1 J3001 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	VBATT		2	GND
3	VBATT		4	GND
5	VBATT		6	GND
7	VBATT		8	VBUS_USB_IN
9	VBATT		10	VBUS_USB_IN
11	GND		12	VBUS_USB_IN
13	GND		14	GND
15	VREG_LVS2A_1P8		16	VREG_S4A_1P8
17	VPH_PWR		18	VREG_L21A_2P95
19	ALPS_INT_N		20	GND
21	FP_INT		22	MAG_DRDY_INT
23	BLSP6_UART_TX		24	APPS_I2C7_SDA
25	BLSP6_UART_RX		26	APPS_I2C7_SCL
27	BLSP6_I2C_SDA		28	SSC_I2C_2_SDA
29	BLSP6_I2C_SCL		30	SSC_I2C_2_SCL
31	SSC_I2C_3_SDA		32	VBATT_CONN_VSENSE_P
33	SSC_I2C_3_SCL		34	VBATT_CONN_VSENSE_M
35	PCIE1_RST_N		36	RSENSE_EXT_M
37	PCIE1_WAKEUP		38	RSENSE_EXT_P
39	PM_RESIN_N		40	GND
41	KYPD_PWR_N1		42	BAT_THERM

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43	USB_ID	44	GYRO_INT
45	GND	46	PARALLEL_CHG_EN
47	USB1_HS_DP	48	PARALLEL_CHG_SHDN
49	USB1_HS_DM	50	SMB1351_VCHG

5.2 J3002 BTB Connector

Pin	Signal Name	Pin	Signal Name
1	SSC_SPI_1_CLK	2	BLSP9_UART_TX
3	SSC_SPI_1_MOSI	4	BLSP9_UART_RX
5	SSC_SPI_1_CS_N	6	PM_PWM1
7	SSC_SPI_1_MISO	8	PM_PWM2
9	CBL_PWR_N	10	SDC4_D0
11	PMI_MPP1	12	SDC4_D3
13	PM_MPP5	14	SDC4_D1
15	GND	16	SDC4_CMD
17	SDC2_SDCARD_CLK	18	GND
19	SDC2_SDCARD_CMD	20	SDC4_CLK
21	SDC2_SDCARD_D3	22	SDC4_D2
23	SDC2_SDCARD_D2	24	BLSP11_UART_TX
25	SDC2_SDCARD_D1	26	BLSP11_UART_RX
27	SDC2_SDCARD_D0	28	NFC_SPI_ESE_CS
29	SD_CARD_DET_N	30	CODEC_INT1
31	NFC_SPI_ESE_MOSI	32	CODEC_INT2
33	NFC_SPI_ESE_MISO	34	VREG_L22A_2P8
35	NFC_SPI_ESE_CLK	36	SLIMBUS_DATA0
37	GND	38	SLIMBUS_DATA1

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39	USB3_SS_TX0_P		40	SLIMBUS_CLK
41	USB3_SS_TX0_M		42	CODEC_RESET_N
43	GND		44	DIVCLK1_CDC
45	USB3_SS_RX0_P		46	GND
47	USB3_SS_RX0_M		48	USB2_HS_D_P
49	GND		50	USB2_HS_D_M

5.3 J2502 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	GND		2	VBATT
3	PCIE1_REFCLK_N		4	VBATT
5	PCIE1_REFCLK_P		6	GND
7	GND		8	VREG_L19A_3P0
9	PCIE_MSM_RX_N		10	FLASH_LED1
11	PCIE_MSM_RX_P		12	FLASH_LED2
13	GND		14	GREEN_LED
15	PCIE1_MSM_TX_N		16	RED_LED
17	PCIE1_MSM_TX_P		18	HDMI_CEC
19	GND		20	HDMI_DDC_CLK
21	MI2S3_DO		22	HDMI_DDC_DATA
23	MI2S3_MCLK		24	HDMI_HOT_PLUG_DET
25	FP_SPI_CS		26	GND
27	FP_SPI_MOSI		28	HDMI_TX2_M
29	PCIE1_CLKREQ_N		30	HDMI_TX2_P
31	FP_SPI_MISO		32	GND
33	MI2S3_SCK		34	HDMI_TX0_M

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35	MI2S3_DI		36	HDMI_TX0_P
37	FP_SPI_CLK		38	GND
39	MSM_UART_TX		40	HDMI_TX1_P
41	MSM_UART_RX		42	HDMI_TX1_M
43	VPH_PWR		44	GND
45	MI2S3_WS		46	HDMI_TCLK_P
47	VBUS_USB_IN		48	HDMI_TCLK_M
49	VBUS_USB_IN		50	GND

5.4 J2601 Camera Connector

Pin	Signal Name		Pin	Signal Name
1	GND		30	GND
2	GND		29	MIPI_CSIO_LANE1_N
3	CCI_I2C_SDA0		28	MIPI_CSIO_LANE1_P
4	VREG_L23A_2P8		27	GND
5	VREG_LVS1A_1P8		26	MIPI_CSIO_CLK_N
6	CCI_I2C_SCL0		25	MIPI_CSIO_CLK_P
7	GND		24	GND
8	MCAM_PWDN		23	MIPI_CSIO_LANE0_N
9	VREG_L17A_2P7		22	MIPI_CSIO_LANE0_P
10	VREG_L3A_1P1		21	GND
11	MCAM_RST		20	MIPI_CSIO_LANE2_N
12	MCAM1_STOBE		19	MIPI_CSIO_LANE2_P
13	GND		18	GND
14	CAM_MCLK0		17	MIPI_CSIO_LANE3_N
15	GND		16	MIPI_CSIO_LANE3_P

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5.5 J2602 Camera Connector

Pin	Signal Name		Pin	Signal Name
1	GND		30	GND
2	GND		29	MIPI_CSI1_LANE1_N
3	CCI_I2C_SDA0		28	MIPI_CSI1_LANE1_P
4	VREG_L23A_2P8		27	GND
5	VREG_LVS1A_1P8		26	MIPI_CSI1_CLK_N
6	CCI_I2C_SCL0		25	MIPI_CSI1_CLK_P
7	GND		24	GND
8	SMCAM1_POWDN		23	MIPI_CSI1_LANE0_N
9	VREG_L16A_2P7_RCM		22	MIPI_CSI1_LANE0_P
10	VREG_WTR_1P0		21	GND
11	SMCAM_RESET		20	MIPI_CSI1_LANE2_N
12	SMCAM_STOBE		19	MIPI_CSI1_LANE2_P
13	GND		18	GND
14	CAM_MCLK1		17	MIPI_CSI1_LANE3_N
15	GND		16	MIPI_CSI1_LANE3_P

5.6 J2603 Camera Connector

Pin	Signal Name		Pin	Signal Name
1	GND		30	GND
2	GND		29	MIPI_CSI2_LANE1_N
3	CCI_I2C_SDA1		28	MIPI_CSI2_LANE1_P
4	VREG_L23A_2P8		27	GND
5	VREG_LVS1A_1P8		26	MIPI_CSI2_CLK_N

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6	CCI_I2C_SCL1	25	MIPI_CSI2_CLK_P
7	GND	24	GND
8	SCAM_PWDN	23	MIPI_CSI2_LANE0_N
9	VREG_L29A_2P8	22	MIPI_CSI2_LANE0_P
10	VREG_WTR_1P0	21	GND
11	SCAM_RESET_N	20	MIPI_CSI2_LANE2_N
12	SCAM_STOBE	19	MIPI_CSI2_LANE2_P
13	GND	18	GND
14	CAM_MCLK2	17	MIPI_CSI2_LANE3_N
15	GND	16	MIPI_CSI2_LANE3_P

Notes: It can be configured as HDMI IN.

5.7 J2510 Display Connector

Pin	Signal Name	Pin	Signal Name
1	GND	27	MIPI_DSI1_LANE1_N
2	MIPI_DSI0_LANE3_N	28	GND
3	MIPI_DSI0_LANE3_P	29	MIPI_DSI1_LANE0_N
4	GND	30	MIPI_DSI1_LANE0_P
5	MIPI_DSI0_LANE2_N	31	GND
6	MIPI_DSI0_LANE2_P	32	LCD_RESET_2
7	GND	33	LCD_CABC
8	MIPI_DSI0_CLK_N	34	LCD_RST_N
9	MIPI_DSI0_CLK_P	35	LCD_TE0
10	GND	36	VREG_DISN
11	MIPI_DSI0_LANE1_N	37	VREG_DISP
12	MIPI_DSI0_LANE1_P	38	VREG_L14A_1P8
13	GND	39	VREG_L18A_2P85

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14	MIPI_DSI0_LANE0_N		40	GND
15	MIPI_DSI0_LANE0_P		41	VREG_WLED
16	GND		42	VREG_WLED
17	MIPI_DSI1_LANE3_N		43	LCD_BL_LED_K1
18	MIPI_DSI1_LANE3_P		44	LCD_BL_LED_K2
19	GND		45	LCD_BL_LED_K3
20	MIPI_DSI1_LANE2_P		46	LCD_BL_LED_K4
21	MIPI_DSI1_LANE2_N		47	GND
22	GND		48	TP_I2C_SDA
23	MIPI_DSI1_CLK_P		49	TP_I2C_SCL
24	MIPI_DSI1_CLK_N		50	BLSP12_UART_TX
25	GND		51	BLSP12_UART_RX
26	MIPI_DSI1_LANE1_P			

Notes:

This VREG_WLED pin only is used to TFT LCD backlight, not OLED LCD

5.8 CON5 Key FPC Connector

Pin	Signal Name	Pin	Signal Name
1	KYPD_PWR_N1	5	KEY_HOME_N
2	GND	6	KEY_BACK_N
3	PM_RESIN_N	7	KEY_GPIO
4	KEY_VOL_UP_N	8	GND

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6 Mechanical Size

6.1 Mechanical Size

The size of Thundersoft TurboX® S820 SOM is 40 x 55mm. Thickness is 5.5mm. You can check the size of BTB connectors through their datasheets.

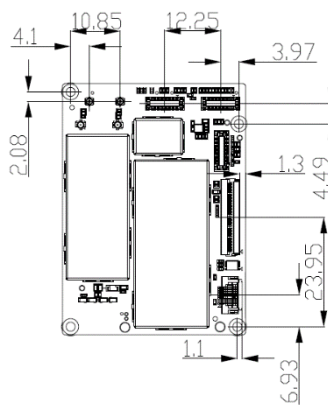


Figure 5-6.1-3 Top View

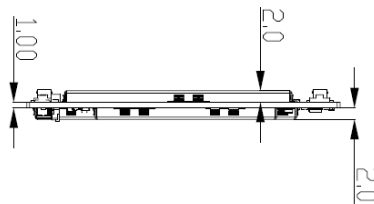


Figure 5-6.1-2 Side View

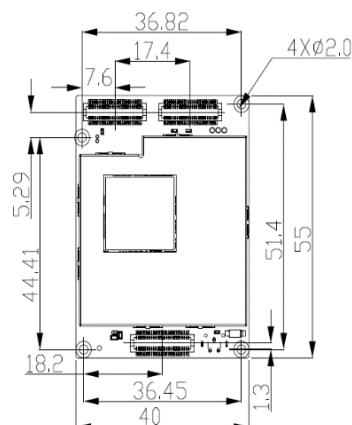


Figure 5-6.1-1 Bottom View